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Colour TV
Service Manual

Model: 29WHP3/ANZ
Chassis: UOC-TDA9384

CONTENT

THE MAIN CHIPS TDA9384/TDA9363

The UOC ("Ultimate One Chip") TDA9363 is adopted in this chassis. This IC is the first available component that contains the complete control and small signal functionality needed for a TV application in one device.

1. The UOC TDA9363 pins function description: (total 64 pins)

Pin1:	Standby control,"1" is on,"0"is off.
Pin2:	SCL.
Pin3:	SDA.
Pin4:	Tuning PWM output.
Pin5:	Auto AV control SW, connected with the SCART2's 8th pin. Input. The rising edge or the falling edge operates.
Pin6:	Key board input.
Pin7:	Mute control, "1" is mute, "0"is off.
Pin8:	CTL, the earth magnetic field rectification output.
Pin9:	Pin12, Pin18, Pin30, Pin35, Pin41, Pin55: GND.
Pin10:	LED, the lamp control output. "1" is on standby, the lamp is light, "0" is turn-on. The lamp is dim.
Pin11:	RELAY, control the K701,"1"is degaussing,"0"is not.
Pin13:	SECAM PLL connected with a capacitance.
Pin14:	+8V power source supply
Pin15:	Using a capacitor of 220n in series to GND, This pin decouples the internal digital supply voltage of the video processor and minimizes the disturbance to the sensitive analogue parts.
Pin16:	PHI-2 control loop, this pin requires a capacitor at 2.2nF (C) in series to GND.
Pin17:	PHI-1 control loop, the loop filter connected to pin 17 is suitable for various signal conditions like strong/weak and VCR signal. This is achieved by switching of the loop filter time constant by changing the PHI-1 output current.
Pin18:	GND.
Pin19:	Bandgap decoupling, the bandgap circuit provides a very stable and temperature independent reference voltage. This reference voltage (4.0 V) ensures optimal performance of the analogue video processor part of the TDA9363 and is used in almost all functional circuit blocks.
Pin20:	East-west pillow signal output.
Pin21:	Vertical drive output.
Pin22:	
Pin23:	IF input.
Pin24:	
Pin25:	Reference current, This pin requires a resistor to ground. The optimal reference current is 100mA, which is determined by this resistor. The 100mA reference current should not be changed because the geometry processor is optimised for this current. Furthermore the output current of vertical drive and EW are proportional to this current.
Pin26:	Vertical sawtooth, This pin requires a capacitor to ground of 100nF.
Pin27:	AGC output. This output is used to control (reduce) the tuner gain for strong RF signals.
Pin28:	Audio de-emphasis.

Pin29:	Sound decoupling. This pin requires a capacitor connected to ground. The pin acts as a low pass filter needed for the DC feedback loop.
Pin30:	GND.
Pin31:	Sound loop filter.
Pin32:	AVL filter.
Pin33:	Horizontal drive signal output, needs a resistor in series to +8V.
Pin34:	Sandcastle output/flyback input
Pin35:	External audio input, this pin should be grounded in this chassis.
Pin36:	EHT tracking/ overvoltage protection. If something is wrong, the anode high voltage rises, the heater voltage will rise too. When the rising voltage arrive some limit, the V406 works, the voltage of pin 36 will exceed 3.9V, the TDA9363 will stop working.
Pin37:	PLL loop filter.
Pin38:	CVBS output. Monitor or RF videos can be selected.
Pin39:	+8V supply source.
Pin40:	CVBS input
Pin42:	Y signal input.
Pin43:	C signal input.
Pin44:	Main audio output, this pin is connected to the TDA9859.
Pin45:	RGB signal input blanking.
Pin46, Pin47, Pin48:	RGB signal input.
Pin49:	ABL. It means been current limiter input. The R410 is the control resister.
Pin50:	Black current input from the CRT board.
Pin51, Pin52, Pin53:	RGB drive signal output to the CRT board.
Pin54:	+3.3V.
Pin55:	GND.
Pin56:	+3.3V.
Pin57, Pin58, Pin59:	12MHz crystal.
Pin60:	Reset, NC in this chassis.
Pin61:	+3.3V
Pin62:	NC.
Pin63:	This pin is connected to the HEF4094, Functions expanding.
Pin64:	IR signal input.

2. Memory AT24C08 is an E^2PROM of 8k, pins describe as follows:

Pin1, Pin2, Pin4, Pin7:	GND.
Pin3, Pin8:	+5V-1 supply.
Pin5:	SDA.
Pin6:	SCL.

3. HEF4094B is described as follows:（total 16 pins）

Pin1:	Connected with UOC Pin63.
Pin2:	SDA.
Pin3:	SCL.
Pin4, Pin5:	AV control switch output, connected to the HEF4052. Data as follows: HEF4094B Pin5 / HEF4052 Pin9 | HEF4094B Pin4 / HEF4052 Pin10 | STATE 0 | 0 | AV1 1 | 0 | AV2 0 | 1 | AV3 1 | 1 | SVHS
Pin8:	GND.
Pin11, Pin12:	Tuner bands control output. Data as follows: HEF4094B Pin11 | HEF4094B Pin 12 | Band 0 | 0 | VHF—L 1 | 0 | VHF—H 0 | 1 | UHF
Pin14:	NC.
Pin15:	Control port, it is high level in this chassis.
Pin16:	+5V supply.

SIGNAL PROCESS

The main chip is N201 TDA9363, AV control switch HEF4052, sound process chip is TDA9859, sound driver is N601 TDA7495S.

The TV signal inputs into the tuner (U101) from CABLE or antenna. The pin 11 and pin 12 of the N502 are combined to select the band. The pin 4 of the N201 outputs the PWM tuning signal. The IF video signal comes from the IF pin of the tuner. The 38.9MHz IF signal is coupled to the N101 (pre-amplify) and then to SAWF (Z101). After processed in the SAWF, the 38.9MHz signal gets to the pin 23 and pin 24 of TDA9363. The IF circuit in TDA9363 includes such unit as the AGC amplifying circuit, 38.9MHz oscillator, PLL video demodulator, video amplifier, IF identify circuit and AFT circuit. The demodulated signal (CVBS) comes from the pin 38 of TDA9363, the sound signal comes from the pin 44.

The internal CVBS signal needs norm identification then outputs from the pin 38 of TDA9363, via the trap-wave circuit (composed of the V504, Z501, Z502, Z503, V506 and so on) feeds back to the pin 40 of TDA9363. The RGB signal comes from the pin51, Pin52, Pin53 of TDA9363, and outputs to the CRT board.

The V901, V902 and V903 are the R、G、B drive transistors. The V904, V905, V906, V907, V908, V909 are the auto low bright balance level output circuit, and generate the low bright level current into the pin 50 of TDA9363.

The internal sound signal comes from the pin 44 of TDA9363, via the coupling capacitor C224 connects to the pin 3 and 5 of TDA9859. The TDA9859 is the audio effect processor, the TDA9495S is the driver. The TDA9859 includes bass, treble, balance, surround, effect shortcut options.

THE HORIZONTAL AND VERTICAL CIRCUIT

Through Synchronous separating circuit, the video signal is divided into horizontal-Synchronizing signal and Vertical-Synchronizing signal. The horizontal-Sync pulse coming from the pin 33 is transferred to the horizontal-drive transistor, and will be used to drive the horizontal-transformer. The horizontal-switch transistor is V405, it and the +B supply drives the flyback transformer to generate the anode high voltage, the focus voltage, the screen voltage, the CRT board drive voltage 190V, the vertical drive voltage 17V and 54V.

The East-west pillow signal comes from the pin 20 of TDA9363. The wave is amplified to modulate the horizontal drive circuit. The amplifying circuit composed of the V401, V403, V402 and other peripheral parts.

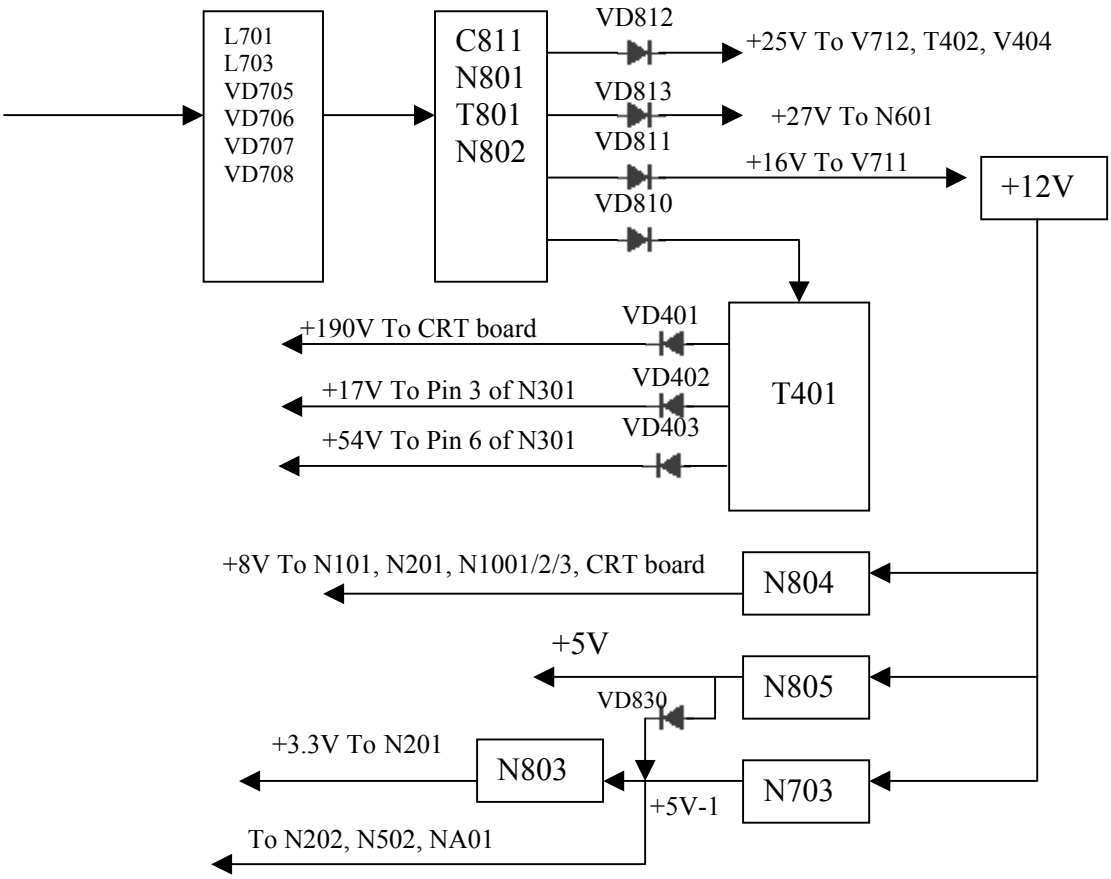
The vertical sawtooth wave is generated on the pin 21 and 22, and then enters the vertical output amplifier circuit. The vertical output amplifier circuit is realized with the power amplifier IC – TDA8351.

The TDA8351 is a 9 pins vertical deflection circuit (3 Amperes) for DC-coupled 90° or 110°deflection systems with frame frequencies from 50 up to 120 Hz. Only a single supply voltage for the scan and a second supply for the flyback are needed.

The vertical drive currents of TDA9363 pins 21 and 22 are connected to input pins 1 and 2 of the TDA8351. The currents are converted into a voltage by resistor R305. Pin 2 is on a fixed DC level (internal bias voltage, about 2.3V) and on pin 1 the drive voltage can be measured (typical 1.4 Vpp). The outputs (pins 4 and 7) are connected to the series connection of the vertical deflection coil and feedback resistor R306 and R308. The voltage across R306 and R308 is fed via pin 9 to obtain a deflection current which is proportional to the drive voltage. The supply voltage for the TDA8351 is 17V at pin 3. The flyback generator has a separate supply voltage of 54V on pin 6. On pin 8 a vertical guard signal is available. For HF loop stability a damping resistor R309 is connected across the deflection coil.

POWER SUPPLY

The IC of KA5Q1265RF is adapted in this chassis; it is the product of Fairchild. It supplies four DC voltages, one is the +B═130V, another is Hcc═25V, the third is 27V (the sound drive voltage), the fourth is +16V. The +16V can generate the +8V, +5V and +3.3V by the special generators.
Fig.2 The power supplies illustration.



FACTORY MODE

SC-1033 UOC factory menu 1	Value	Description	M
PARA5/6 (50H/60H)	31	Parallelogram	🛠
BOW5/6 (50H/60H)	31	Bow	🛠
HPS5/6 (50H/60H)	31	Horizontal center	🛠
WID5/6 (50H/60H)	31	Width	🛠
DPC5/6 (50H/60H)	31	Parabola	🛠
UCNR5/6 (50H/60H)	31	Up-corner	🛠
LCNR5/6 (50H/60H)	31	Low-corner	🛠
KEY5/6 (50H/60H)	31	Trapezium	🛠
SC-1033 UOC factory menu 2	**Value**	**Description**	**M**
VLIN5/6 (50H/60H)	31	Vertical linearity	🛠
HIT5/6 (50H/60H)	31	Vertical amplitude	🛠
VSC5/6 (50H/60H)	31	Vertical S-correction	🛠
VP50/60 (50H/60H)	31	Vertical center	🛠
OSDV5/6 (50H/60H)	31	OSD vertical position	🛠
VX	30	Vertical amplify	ⓘ
RCUT	31		🛠
GCUT	31		🛠
SC-1033 UOC factory menu 3	**Value**	**Description**	**M**
RDRV	31		🛠
GDRV	31		🛠
BDRV	31		🛠
WBBRI	31		ⓘ
WBCON	60		ⓘ
LANG	4	OK language option	ⓘ
YDFP	7	Y-delay: SECAM/PAL/NTSC individually	ⓘ
AGC	28		ⓘ

SC-1033 UOC factory menu 4	Value	Description	M
VOL	20	TDA9859 volume	🛠
9874	10	TDA9874AH volume	ⓘ
IFFS	2	IF option	ⓘ
HDOL	8	Cathode inspect level	ⓘ
AGCS	1	AGC operate speed	ⓘ
VG2B	39	Screen adjust state	ⓘ
TILT	31		🛠
VX16	2	Vertical amplify in 16:9 state	🛠
SC-1033 UOC factory menu 5	**Value**	**Description**	**M**
OSDL	0	OSD bright	ⓘ
BCF	2	Start time in M state	ⓘ
OKBCF	4	Start time in OK state	ⓘ
BRI50/60 (50H/60H)	39	Sub-bright	🛠
CON50/60 (50H/60H)	61	Sub-contrast	🛠
COL50/60 (50H/60H)	61	Sub-color	🛠
SHA50/60 (50H/60H)	31	Sub-sharpness	🛠
HUE50/60 (50H/60H)	50	Sub-tint	🛠
SC-1033 UOC factory menu 6	**Value**	**Description**	**M**
OPT1	204	Refer to Table 3	ⓘ
OPT2	3	Refer to Table 3	ⓘ
OPT3	115	Refer to Table 3	ⓘ
OPT4	243	Refer to Table 3	ⓘ
OPT5	55	Refer to Table 3	ⓘ
OPT6	127	Refer to Table 3	ⓘ
INIT		Reset	ⓘ

M legend explain:
🛠 : Manufacture adjusting item
ⓘ : Soft relative items

M state entrance process:
quickly step by step press the key mute, call and 980.

Option of menu 6

OP_DEFAULT_OPT_1	0x098	/*	VG2 mode	No
			Comb filter	No
			Super woofer	No
			AV3	Yes
			SVHS	Yes
			DVD	No
			RGB	No
			OSO	Yes */
OP_DEFAULT_OPT_2	0x003	/*	AVL	Yes
			Auto Sound	Yes
			National Option table 1	No
			National Option table 2	No
			National Option table 2	No
			Function 1	No
			Function 2	No
			FSL	No */
OP_DEFAULT_OPT_3	0x0F3	/*	AFC_SAVING	Yes
			NV_8598	Yes
			CHARGING	No
			SECAM_SVM	No
			Sound DK	Yes
			Sound BG	Yes
			Sound I	Yes
			Sound M	Yes */
OP_DEFAULT_OPT_4	0x0FB	/*	FMWS	Yes
			Direct switch on	Yes
			AKB	No
			LOGO	Yes
			HCO	Yes
			IDENT_SENSITIVE	Yes
			STABLE	Yes
			DFL	Yes */
OP_DEFAULT_OPT_5	0x03F	/*	TILT	Yes
			NICAM	Yes
			BOX	Yes
			MONITOR	Yes
			CALENDAR	Yes
			GAME	Yes
			RESERVED	No
			ZOOM 16:9 OSVE	No */

OP_DEFAULT_OPT_6	0x07F	/*	ENGLISH	YES
			SPANISH	YES
			ARABRIC	YES
			GERMAN	YES
			FRENCH	YES
			ROMANIAN	YES
			TURKISH	YES
			RUSSIAN	NO */
OP_DEFAULT_OPT_7	0x00D	/*	OP_FARSI	YES
			OP_MALAYSIA	No
			OP_ITALIAN	YES
			OP_HUNGARY	YES
			OP_MAGNETIC	
			OP_HOTEL	NO
			OP_AGCL1	NO
			OP_AGCL2	NO */
OP_DEFAULT_OPT_8	0x004	/*	OP_BBSW	NO
			OP_BLACK_BACK	NO
			OP_CURTAIN	YES

APPENDIX

HEF4052B illustration

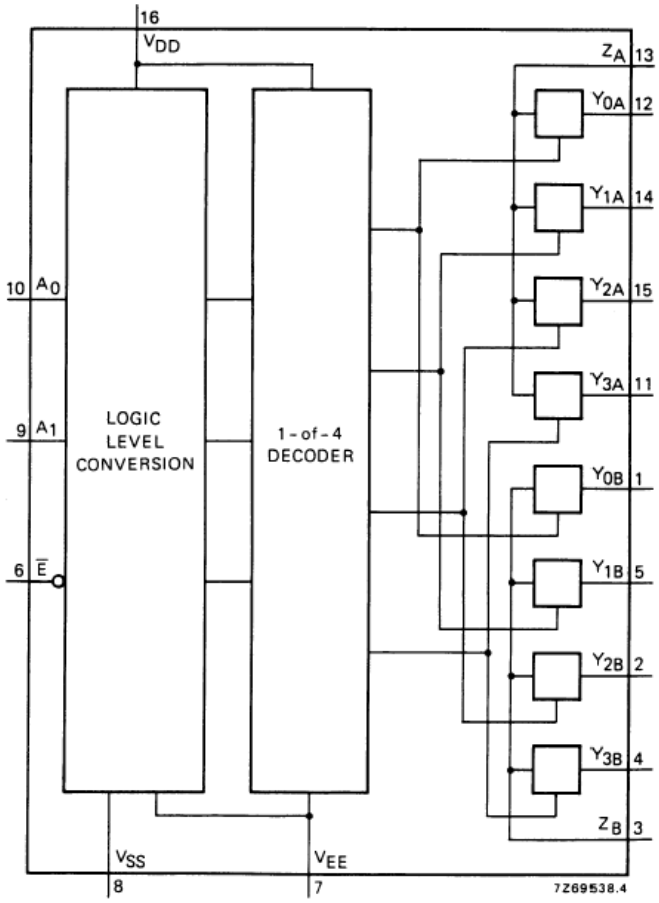


Fig.1 Functional diagram.

PINNING

Y_{0A} to Y_{3A}	independent inputs/outputs
Y_{0B} to Y_{3B}	independent inputs/outputs
A_0, A_1	address inputs
$\overline{E}$	enable input (active LOW)
Z_A, Z_B	common inputs/outputs

FAMILY DATA,
I_{DD} LIMITS category MSI

See Family Specifications

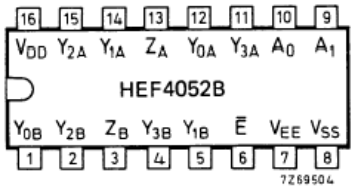


Fig.2 Pinning diagram.

HEF4052BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4052BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4052BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

TDA9859 illustration 1

PINNING

SYMBOL	PIN	DESCRIPTION
$SCIN_L$	1	SCART input; left channel
P1	2	port 1 output
MIN_L	3	MAIN input; left channel
C_{SMO}	4	smoothing capacitor of reference voltage
MIN_R	5	MAIN input; right channel
V_P	6	supply voltage
$SCOUT_R$	7	SCART output; right channel
GND	8	ground
$MOUT_R$	9	MAIN output; right channel
LIN_R	10	input to right loudspeaker channel
C_{BR1}	11	bass capacitor connection 1; right channel
C_{BR2}	12	bass capacitor connection 2; right channel
n.c.	13	not connected
C_{TR}	14	treble capacitor connection; right channel
$LOUT_R$	15	loudspeaker output; right channel
SCL	16	serial clock input; I^2C-bus
SDA	17	serial data input/output; I^2C-bus
$LOUT_L$	18	loudspeaker output; left channel
C_{TL}	19	treble capacitor connection; left channel
n.c.	20	not connected
C_{BL2}	21	bass capacitor connection 2; left channel
C_{BL1}	22	bass capacitor connection 1; left channel
LIN_L	23	input to left loudspeaker channel
$MOUT_L$	24	MAIN output; left channel
MAD	25	module address select input
$SCOUT_L$	26	SCART output; left channel
C_{PS2}	27	pseudo stereo capacitor 2
AIN_L	28	AUX input; left channel
C_{PS1}	29	pseudo stereo capacitor 1
AIN_R	30	AUX input; right channel
P2	31	port 2 output
$SCIN_R$	32	SCART input signal RIGHT

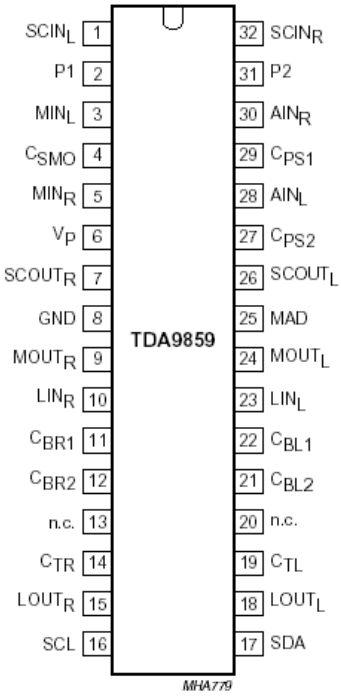
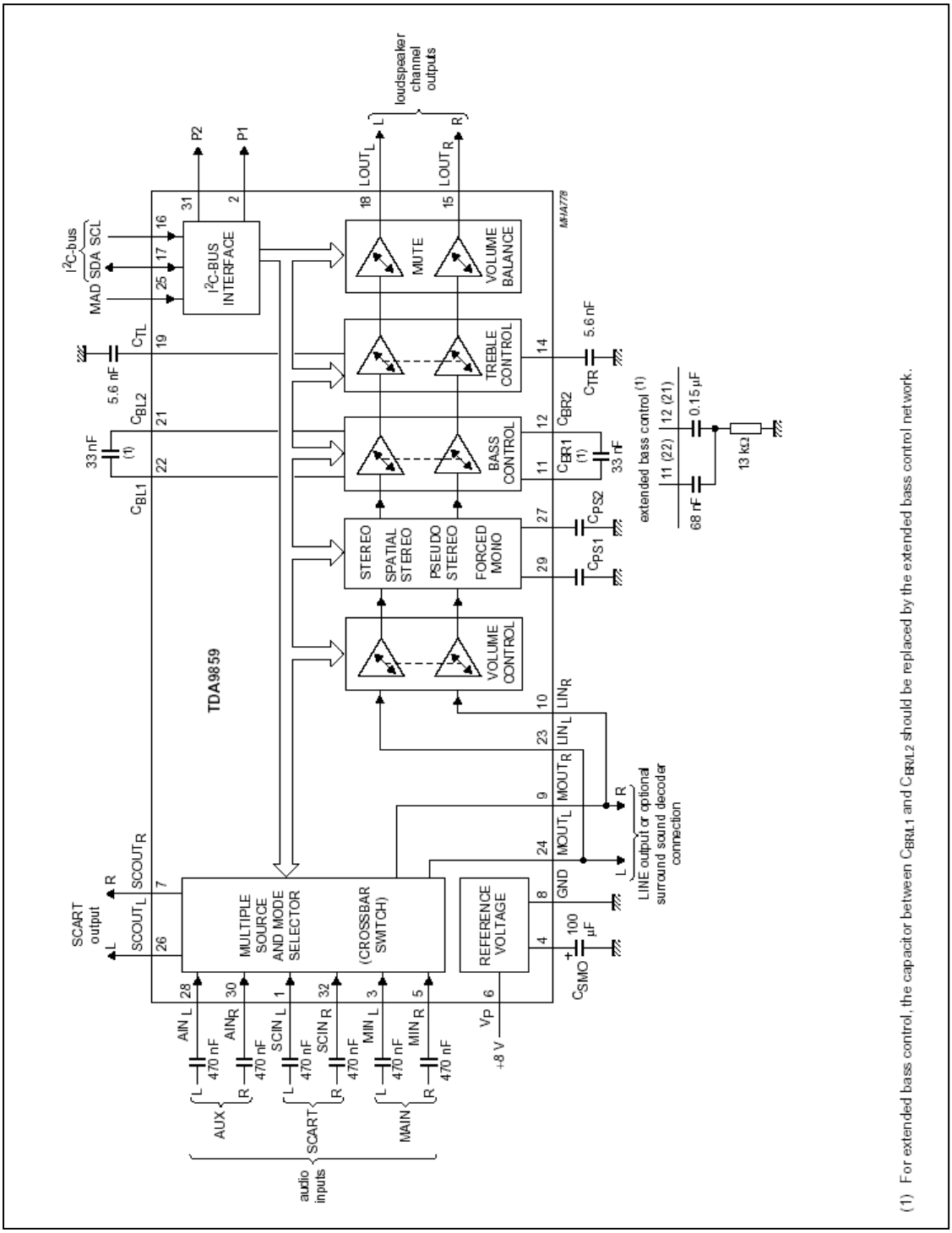
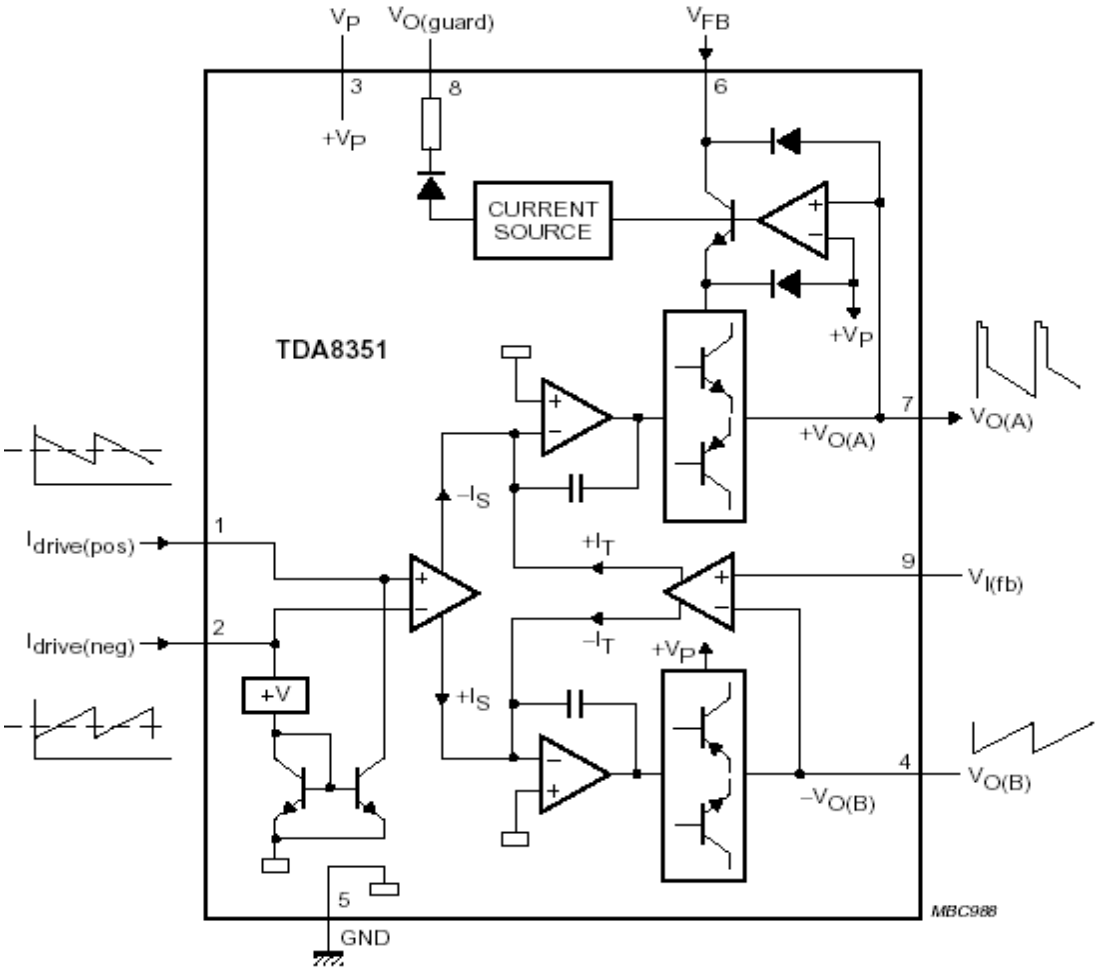


Fig.2 Pin configuration.

TDA9859 illustration 2

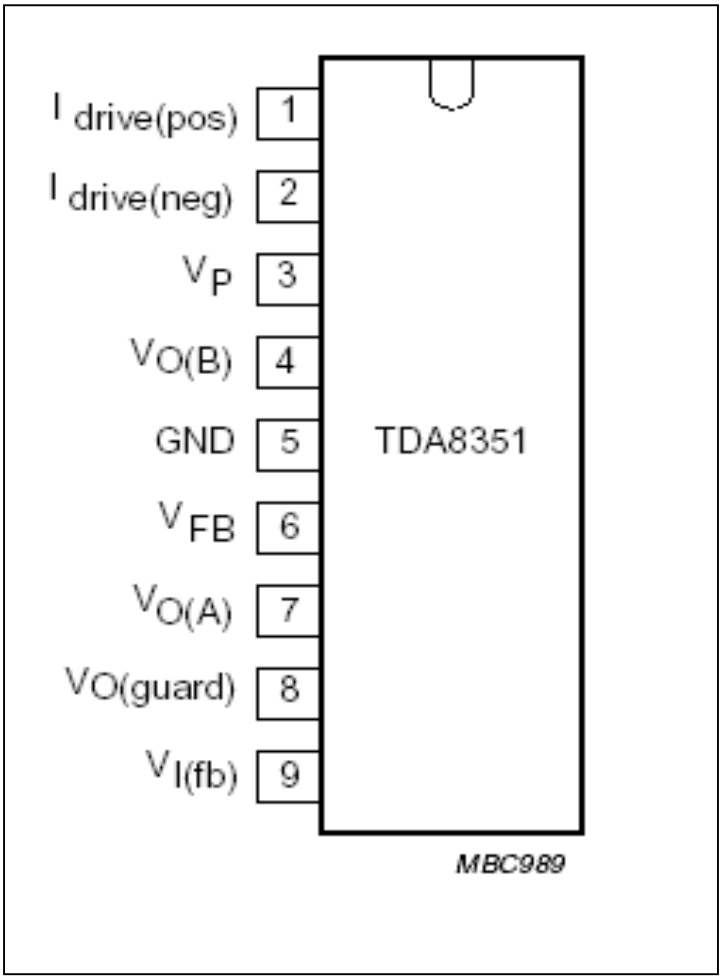


TDA8351 illustration 1

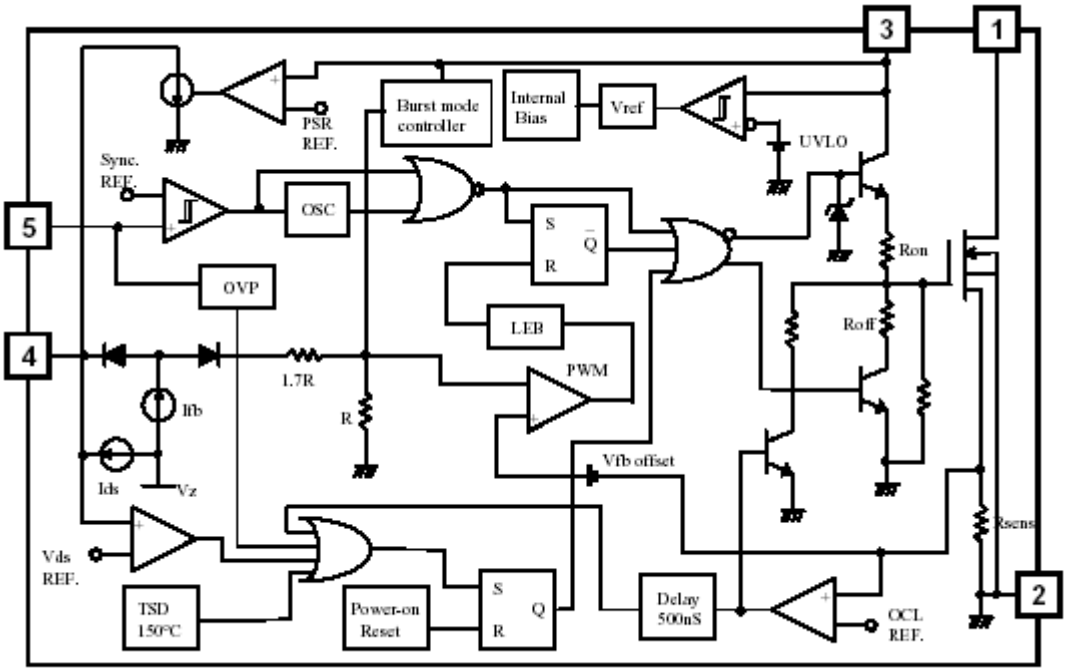


TDA8351 illustration 2

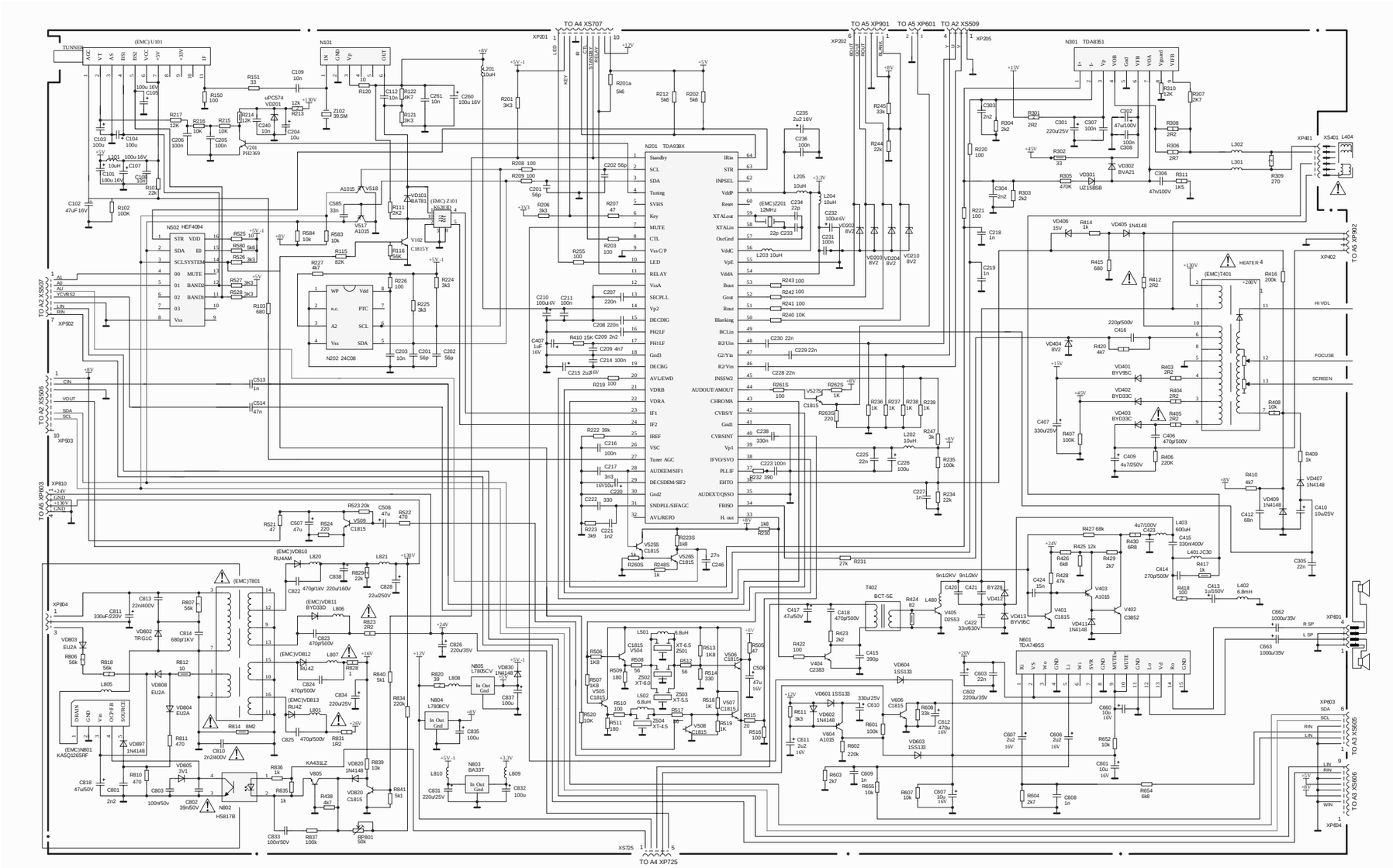
SYMBOL	PIN	DESCRIPTION
$\|_{drive\ (pos)}$	1	Input power-stage (positive); Includes $\|_{(sb)}$ signal bias
$\|_{drive\ (neg)}$	2	Input power-stage (negative); Includes $\|_{(sb)}$ signal bias
Vp	3	Operating supply voltage
$V_{O(B)}$	4	Output voltage B
GND	5	Ground
V_{FB}	6	Input flyback supply voltage
$V_{O(A)}$	7	Output voltage A
$V_{O(guard)}$	8	Guard output voltage
$V_{I(fb)}$	9	Input feedback voltage



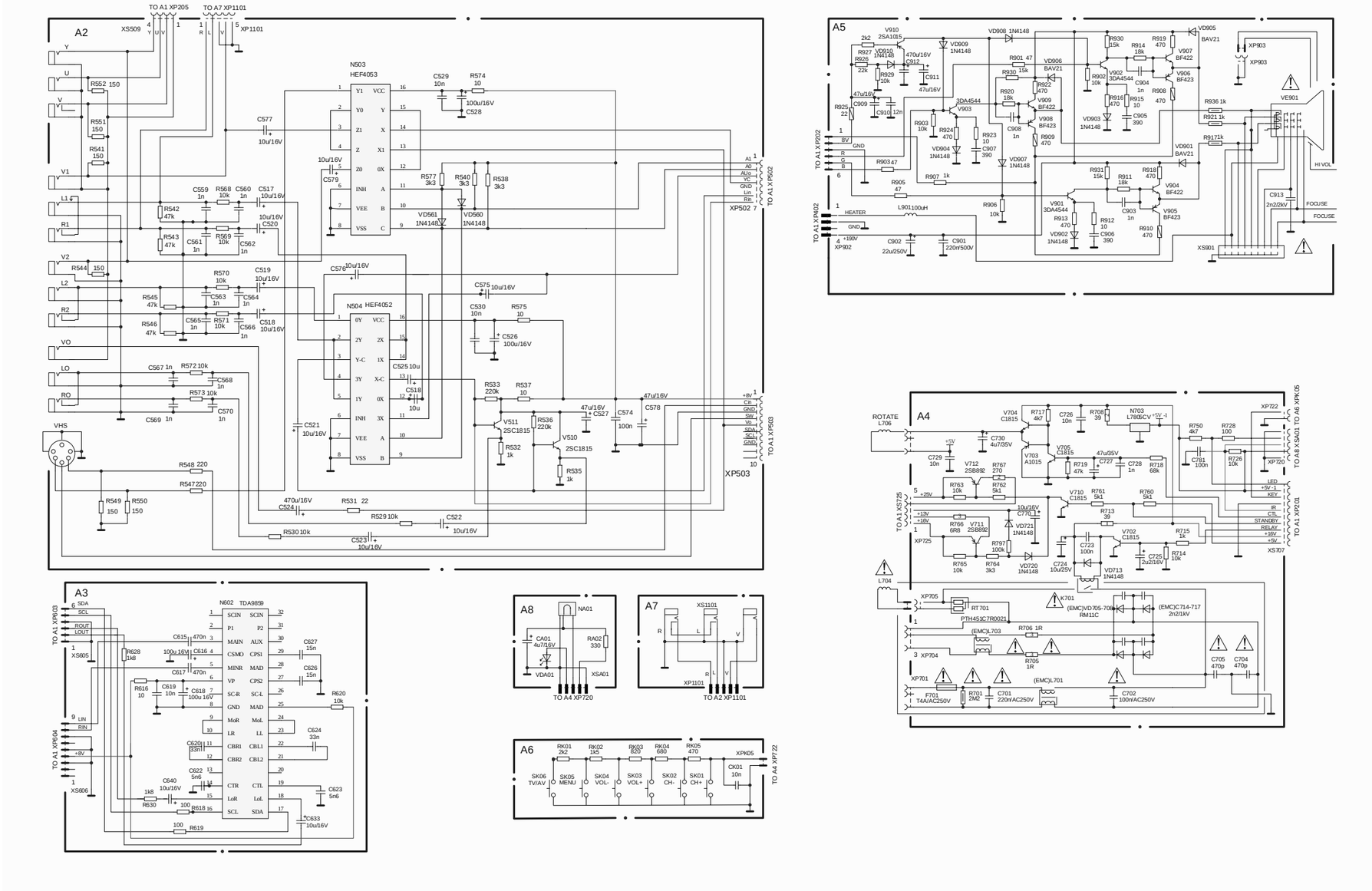
KA5Q1265RF illustration



CIRCUIT DIAGRAM



Note: This circuit diagram covers a basic or representative chassis only. There may be some component or partial circuit differences between the actual chassis and the circuit diagram.



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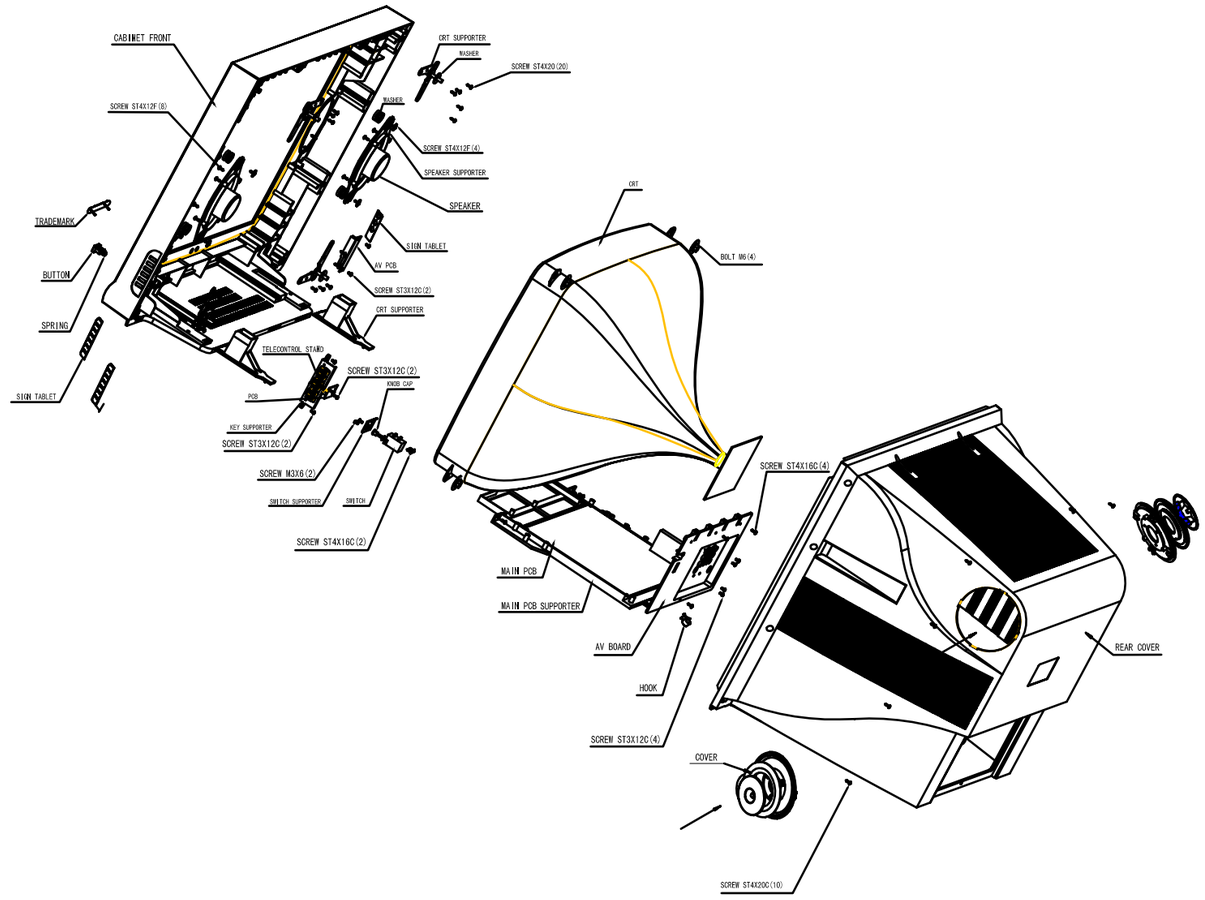
EXPLODED VIEW AND PART NAME



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